IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

TRANSIMPEDANCE AMPLIFIER

RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Patent Application Serial No. 60/463,041 filed April 16, 2003, and entitled "Transimpedance Amplifier".

TECHNICAL FILED OF THE INVENTION

[0002] The present invention relates to transimpedance amplifiers, and more particularly to a transimpedance amplifier having improved linear operating characteristics.

BACKGROUND OF THE INVENTION

[0003] There are many systems applications where an accurate conversion of an input current to a voltage output is required. This process is called Transimpedance Amplification (TA). In addition, the source of signal current may be a sensor element (such as, for example, a photodiode) in which the voltage across the photodiode must be held to a value as close to 0 volts as possible to minimize error producing leakage currents. The use of an operational amplifier (OA) to hold the voltage across the sensor element at 0 Volts (0V) with a feedback resistor converts the signal current to a voltage.

[0004] As is true with most sensor interface problems, the requirement exists to maximize the Signal-to-Noise (SIN) ratio due to the need to detect smaller and smaller signal currents. This drive toward higher sensitivity implies the need to implement increasingly larger values of the feedback resistor. In tandem, there is always the desire to maximize the accuracy of the sensor as well as to increase its bandwidth. This desire results in the need for the feedback resistor to be as linear as possible over its operating voltage and temperature range and for its implementation to minimize any parasitic

elements. Finally, the requirement to package this high sensitivity TA in as small a volume as possible due to the physical placement of the sensor into tight locations exists. This miniaturization requirement leads to the need to implement a self contained TA in integrated circuit form.

[0005] In an integrated circuit TA the physical size of the resistance element presents a problem. If implemented with available on-chip resistors, this resistor will become physically quite large to the point of increasing cost to an unfeasible level for all but the lowest sensitivity applications. In response to this problem a metal-oxide-semiconductor (MOS) transistor as a resistor based on the knowledge that a MOS device is effectively a voltage controlled resistor when operated in its triode region has been used in TA circuits.

[0006] MOS parameters include surface mobility (μ),gate capacitance (Cox), width (W) and length (L). The combination of MOS parameters sets the maximum resistance the device can exhibit and the externally generated control signal (Vg) is then used to modulate the resistance to a lower value as required. This modulation can be used to counteract temperature effects and MOS device non-linearity.

[0007] A non-linearity that must be dealt with in a TA implementation using a MOS device is saturation. The drain saturation voltage (Vdsat) limits the usable range of output voltage for a particular value of Vgs. This problem can be a significant problem in low voltage circuits, and can be addressed using a voltage divider circuit to scale the drain voltage (Vds) of the MOS device to a value that is within its linear range.

[0008] An additional non-linearity to be overcome centers on the Vds vs Ids characteristic of the MOS device while the device is operating within its triode region. If the TA is to be operated under constant Vgs conditions, the value of Vgs will have to be very large when compared to the device's Vds. Assuming constant Vgs operation, this operation also means that the W/L of the device will have to be reduced as the value of Vgs is increased such that the product of (Vgs-Vto) X (W/L) remains constant. This geometric ratio increase will increase the MOS device's gate area which will decrease its

bandwidth capability. The trade here is to increase the voltage divider ratio, but this will significantly increase the offset error term in most cases.

[0009] Taking all of the above trade factors into consideration, the concept of implementing an integrated circuit TA using an MOS device under constant Vgs bias as the resistance element is considered to be impractical in many cases except those in where accuracy is not a primary requirement. To solve this problem, the use of a variable gate bias as a function of the input signal current has been developed. The gate bias is derived and is modulated by the output voltage of the TA. However, a need still exists for a TA with highly linear operation.

SUMMARY OF THE INVENTION

[00010] In accordance with the present invention, a transimpedance amplifier is provided. The transimpedance amplifier includes a first amplifier, a first MOS resistor device and a first voltage divider circuit. The source terminal of the first MOS resistor device is coupled to the first amplifier inverting input. The voltage divider circuit is coupled between the first amplifier output and the non-inverting input. The output of the first voltage divider is coupled to the first MOS resistor drain terminal. A second amplifier, second MOS resistor device and a second voltage divider circuit is also provided. The output of the second amplifier is coupled to the gate terminal of the first MOS resistor device. The gate terminal of the second MOS resistor device is coupled to the second amplifier output. The drain terminal of the second MOS resistor device is coupled to the second amplifier non-inverting input. The second voltage divider circuit is coupled between the first amplifier output and the second MOS resistor device source terminal, and has an output coupled to the second amplifier inverting input.

BRIEF DESCRIPTION OF THE DRAWINGS

[00011] For a more complete understanding of the present invention and for further advantages thereof, reference is now made to the following Description of the Preferred Embodiments taken in conjunction with the accompanying Drawings in which:

FIG. 1 is a schematic diagram of the present transimpedance amplifier; and

FIG 2 is a schematic diagram of an alternate embodiment of the present transimpedance amplifier.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[00012] Referring to FIG. 1, the present transimpedance amplifier is illustrated, and is generally identified by the numeral 10. Transimpedance amplifier circuit 10 utilizes an operational amplifier circuit, generally identified by the numeral 12 and a gate bias circuit, generally identified by the numeral 14.

[00013] Operational amplifier circuit 12 includes an operational amplifier 20 (OA1) having an inverting input 22, a non-inverting input 24 and an output 26. A source of signal current is provided by a sensor element, such as for example, photodiode 28 (D1) which generates current I_s.

[00014] Coupled to output 26 of operational amplifier 20 is a voltage divider circuit, generally identified by the numeral 30. Voltage divider circuit 30 includes a resistor 32 (R1) and a resistor 34 (R2) and has an output 36.

[00015] A MOS resistor device, generally identified by the numeral 40 (MN1) is coupled between the output 36 of voltage divider circuit 30 and the inverting input 22 of operational amplifier 20. MOS resistor device 40 includes a drain terminal 42, source terminal 44 and gate terminal 46. The gate bias V_g is modulated by the output voltage of operational amplifier 20 utilizing gate bias circuit 14.

[00016] Gate bias circuit 14 includes an operational amplifier 60 (OA2) having an inverting input 62, a non-inverting input 64 and an output 66. Output 66 of operational amplifier 60 is coupled to gate 46 of MOS resistor device 40.

[00017] Coupled to the output 26 of operational amplifier 20 is a voltage divider circuit, generally identified by the numeral 70. Voltage divider circuit 70 includes a resistor 72 (R3) and resistor 74 (R4). The output 76 of voltage divider circuit 70, Vd, is coupled to the inverting input 62 of operational amplifier 60.

[00018] Also coupled to the output 26 of operational amplifier 20 is a voltage divider circuit, generally identified by the numeral 78. Voltage divider circuit 78 includes a MOS resistor device (MN2), generally identified by the numeral 80. MOS resistor device 80 includes a drain terminal 82, source terminal 84 and a gate terminal 86. Coupled to the drain terminal 82 of MOS resistor device 80 is a resistor 88 (R_{ref}). The output of operational amplifier 60 is applied to the gate terminal 86 of MOS resistor device 80. The output of voltage divider circuit 78 is applied to the non-inverting input 64 of operational amplifier 60. A current source (I_{os}) 90 is also applied to the non-inverting input 64 of operational amplifier 60.

[00019] The operation of TA 10 is as follows. Assume that a DC signal current is flowing and that a differential signal current (dIs) is generated that produces an output voltage (dVout) according to:

$$dVout = \mathrm{d}Is \times Rmn1 \times (1 + R1/R2) \qquad (1)$$

where the MOS 40 resistance (Rmn1) is defined by:

$$1/Rmn1 = (W1/\mathrm{L}1) \times \mu \times Cox \times (Vgs - Vto) \qquad (2)$$

where L1 and W1 are the length and width of MN1, μ is the surface mobility and Cox is the gate capacitance of MN1.

[00020] The differential Vds of MOS device MNl is:

$$Vdsmn1 = Vout \times (R2/(R1 + R2)) \qquad (3)$$

dVout is also applied to the R3-R4 voltage divider 70 in the gate bias circuit 14 resulting in:

$$dVd\ \mathrm{d}Vd = dVout \times (R4/(R3 + R4)). \qquad (4)$$

The drain 82 of MN2 80 is held at dVd by OA2 60 which results in a differential current flowing through Rref of:

$$dlref = (dVout/Rret) \times (R3/(R3 + R4)) \qquad (5)$$

and the resulting resistance of MN2 80 is derived to be:

$$Rmn2 = Rref \times (R4/R3). \qquad (6)$$

[00021] Rmn2 is constant and totally independent of the input voltage (both DC and small signal) and the output of OA2 60 therefore describes the non-linear Vgs voltage required to maintain this resistance level over the total range of Vout. Using this value of resistance, the equation describing Vgs for a particular DC value of Vout can thus be derived to be:

$$Vgs = Vto + (1/Rref) \times (R3/R4)x\ (L2/W2)x\ (1/\mu Cox) \qquad (7)$$

where L2 and W2 are the length and width of MN2, μ is the surface mobility and Cox is the gate capacitance of MN2 80. Substituting this value of Vgs into the Equation (2) for Rmn1 yields:

$$Rmn1 = Rref\ x\ (W2/W1)\ x\ (L1/L2)x\ (R4/R3), \qquad (8)$$

which when substituted back into the Equation (1) describing dVout in terms of Rmn1 yields:

$$dVout = dls \times Rref \times (W2/W1)x(L1/L2) \times (R4/R3)x\ (1 + R1/R2). \qquad (9)$$

Equation (9) is correct if devices 40 and 80 are operated at identical values of Vds. For this operation to be true the R1/R2 and R3/R4 ratios must be identical. Setting these ratios to the value K reduces the Equation (9) to:

$$dVout = dls\ x\ Rref\ x\ (W2/W1) \times (L1/L2) \times (1 + 1/K). \qquad (10)$$

[00022] Equation (10) becomes the governing equation for this configuration which is completely void of any non-linear device parameters. Equation (10) also shows that device scaling applies and that the value of Rref can be reduced by adjusting the MN1 to MN2 geometric ratios.

[00023] Under the condition of zero DC signal current, Vout is zero and all of the drain voltages are 0 which results in a null set of describing equations and a

potentially unstable condition. To alleviate this issue, a small current 90 (Ios) is continuously applied to the drain 82 of MN2 which forces the Vgs output to the voltage required to sink this current and thus ensures continuous operation.

[00024] The transimpedance of the TA 10 is set by resistor Rref 88 and for a totally integrated circuit this resistor must be provided from those available in the process. Rref will therefore have a very large initial tolerance which most likely exceeds the circuit performance requirements. To alleviate this issue a trim procedure is instituted as illustrated in FIG. 2. Inspection of the Vout Equation (10) shows that the geometric ratios between MN1 and MN2 are direct multipliers to the transimpedance. These ratios can therefore be altered to accommodate the Rref tolerance in a manner that keeps the product of Rref and one of the geometric ratios constant. The addition of one or more additional MOS resistor devices 100 in parallel with MOS 80 accomplishes this function.

[00025] Other alteration and modification of the invention will likewise become apparent to those of ordinary skill in the art upon reading the present disclosure, and it is intended that the scope of the invention disclosed herein be limited only by the broadest interpretation of the appended claims to which the inventor is legally entitled.